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| 09/478,714 | 01/06/2000 | TONY S. EL-KIK | BAYS-10-8-2 | 2054 |

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DUANE MORRIS, LLP
ATTN: WILLIAM H. MURRAY
ONE LIBERTY PLACE
1650 MARKET STREET
PHILADELPHIA, PA 19103-7396

| EXAMINER | |
|---|---|
| HUISMAN, DAVID J | |
| ART UNIT | PAPER NUMBER |
| 2183 | |

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/478,714 | EL-KIK ET AL. |
| | Examiner | Art Unit |
| | David J. Huisman | 2183 |

SH

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *25 November 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. Claims 1-16 have been examined.

### *Drawings*

2. The subject matter of this application admits of illustration by a drawing to facilitate understanding of the invention. Applicant is required to furnish a drawing under 37 CFR 1.81. No new matter may be introduced in the required drawing. The Applicant has stated on page 6 of the remarks that Fig.1 has been modified to include an RDN signal and that the new drawing has been submitted. However, the modified version of Fig.1 has not been included with Applicant's response.

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

### *Maintained Rejections*

4. The following 35 U.S.C 103 rejections set forth in the previous Office Action, mailed on August 27, 2002, paper number 3, are respectfully maintained and included below for the convenience of the Applicant.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy et al., U.S. Patent No. 6,085,307 (herein referred to as Evoy) in view of McCarthy et al., U.S. Patent No. 6,321,310 B1 (herein referred to as McCarthy).

7. Referring to claim 1, Evoy has taught a dual processor system, comprising:

a) a first processor coupled to a system address bus and a data bus. See Fig.2.

b) a second processor coupled to the system address bus and to the data bus (see Fig.2), whereby the second processor comprises:

c) a control register having a control register system address. See Fig.2 (57) and column 2, lines 47-52.

d) an internal memory. It is well known in the art that processors contain memory whether it is a RAM, ROM, etc. The memory is used to store instructions or values obtained while executing instructions. In addition, a person of ordinary skill in the art would have recognized that although Evoy has taught communication between two processors through a shared memory source, it is just as plausible to have two processors, each having their own memory to store data/instructions. Then the data transfers would occur directly between the two processors as opposed to a single memory source. One advantage of this scheme is that both processors have access to their respective memories without contention. With a single, shared memory, one processor will have to wait for the other processor to finish before it can access memory, resulting in delayed execution and more time wasted. Therefore, to minimize the time required to access memory, it would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate local, internal memories for each processor.

e) a data register having a data register system address and coupled to the internal memory. See column 5, lines 1-7. Data registers are used to hold intermediate data. In addition, it is well known in the art that data registers are coupled to the processor's internal memory in order to hold data that is to be retrieved from or written to memory.

f) an internal address generator coupled to the control register and to the internal memory. In Evoy's system, the internal control register includes a program counter (see column 5, lines 1-3), which is well known in the art to hold an address of an instruction in memory. Therefore, it would be inherent that an internal address generator would be coupled to the control register and also to the internal memory in order to decode the address being held in the program counter and then access the correct memory address.

g) the control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus. Evoy has taught the connection and interaction between two processors. Evoy did not explicitly teach a burst data transfer between them. However, McCarthy taught a system in which a single or burst data transfer occurs between a first processor and a co-processor before being stored in memory. See Fig.1 and a brief explanation in column 5, lines 61-67 and column 6, lines 1-5. Using the concept of an internal co-processor memory explained above, McCarthy's teachings would be applied to Evoy's system in order to allow the processors to communicate directly with each other without the use of a shared memory. In addition, a person of ordinary skill in the art would have recognized that if a first processor wanted to transfer a burst of data and/or instructions to a second processor, the first processor would have to first inform the second processor of the

desired operating mode in order to prepare the second processor to receive multiple data elements. McCarthy's system uses instructions to implement the single and burst data transfers. See column 5 for examples. It is inherent that the instructions, when decoded and propagated along the data bus, will specify the type of transfer to take place (through a single bit or multiple bits) along with the starting internal address. The concept of McCarthy's system can be applied to Evoy's system such that the second processor will recognize the beginning of a burst transfer (based on the instruction issued by the first processor) and its memory address registers (accessed through the control register, which has an address) will hold the starting internal address. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that in order to store the starting internal address in the memory register of the second processor, the first processor must write the control word to the second processor's control register by applying the control register's address on the address bus and the control word on the data bus.

h) the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode. When the dual processor system is in burst mode, time would be saved by not having the first processor generate a new memory address for each new element it must transfer. McCarthy has taught a burst mode in which the first processor provides the starting address and the co-processor selects consecutive memory addresses for each new data element that it receives. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the

internal address generator of Evoy select consecutive memory addresses as transfers occur. This would allow the first processor to refrain from sending a new address each time, resulting in less computation time.

8. Referring to claim 2, Evoy in view of McCarthy has taught an invention as described in claim 1. Evoy has further taught that the dual processor system is implemented as an integrated circuit. See column 5, lines 52-61, and Fig.2.

9. Referring to claim 3, Evoy in view of McCarthy has taught an invention as described in claim 1. It is inherent that it is undesirable for the second processor to be in burst transfer mode all of the time because it would not have a chance perform floating point or DSP calculations, for example. Therefore, a person of ordinary skill would have recognized that the first processor should provide some sort of signal to the second processor in order to specify the end of burst transfer mode. Since the first processor has already provided the starting address on the address bus at the beginning of burst mode, it would make sense to continue asserting the same address until burst mode is scheduled to end because no extra work would be required by the first processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to have the second processor remain in burst mode as long as the first processor continues to apply the original starting address to the address bus.

10. Referring to claim 4, Evoy in view of McCarthy has taught an invention as described in claim 1. It is well known that when a burst data write takes place, multiple data elements will be involved. In order for the data elements to be transferred and received correctly, they must be processed individually due to the existence of a single data bus. McCarthy has further taught that when transferring data, a buffer is used as an intermediate step to hold multiple data

elements. See Fig.1 (26). A person of ordinary skill in the art would have recognized that a data register would provide the same functionality as a buffer. It would be used to hold data received by the second processor until its memory is available from the previous write. Without the data register (buffer), the first processor would be transferring data directly to the memory of the second processor and because memory is slower than registers, the first processor would have to delay its transfer each time until the memory become available. This would result in less productive work being accomplished and time being wasted. Therefore, in order to achieve a more efficient dual processor system, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first processor write all of its data words to the second processor's data register via the data bus by supplying the data register address on the system address bus. Furthermore, it would be unproductive for the first processor, in addition to transferring each data word, to also calculate and supply a new memory address each time a new word is transferred. A person of ordinary skill in the art would have recognized that since the second processor is currently storing the starting internal memory address, the internal address generator would select consecutive memory locations of the internal memory as new data words are stored.

11. Referring to claim 5, Evoy in view of McCarthy has taught an invention as described in claim 1. It is well known that when a burst data read takes place, multiple data elements will be involved. In order for the data elements to be transferred and received correctly, they must be processed individually due to the existence of a single data bus. McCarthy has further taught that when receiving data, a buffer is used as an intermediate step to hold multiple data elements. See Fig.1 (26). A person of ordinary skill in the art would have recognized that a data register

would provide the same functionality as a buffer. It would be used as intermediate storage to hold data retrieved from the second processor's memory. Without the data register (buffer), the first processor would have to read data directly from the second processor's internal memory. This doesn't pose a big problem but it is rather unproductive. For example, if the data register did not exist as an intermediate storage step, then the first processor would be responsible for reading each value, one at a time, from the second processor's memory. If the first processor needs to perform some other type of work in between reads, it will have to return to memory at a later time to continue with the reads, while the second processor is of no help. On the other hand, if the buffer is implemented and the first processor has to do other work, then the second processor will work to fill the buffer in the meantime as the first processor executes something else. When the first processor is ready to read again, it will simply go to the register file that has been filled with data by the second processor. The advantage is avoiding the time for the first processor to access the internal memory since registers are faster. This would result in a much more productive system. Therefore, in order to achieve a more efficient dual processor system, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first processor read all of the data words from the second processor's data register via the data bus by supplying the data register address on the system address bus. Furthermore, it would be unproductive for the first processor, in addition to transferring each data word, to also calculate and supply a new memory address each time a new word is to be read. A person of ordinary skill in the art would have recognized that since the second processor is currently storing the starting internal memory address, the internal address generator would select consecutive memory locations of the internal memory as new data words are read.

12. Referring to claim 6, Evoy in view of McCarthy has taught an invention as described in claim 1. Evoy has further taught that the second processor is a co-processor. See Fig.2 (50).

13. Referring to claim 7, Evoy in view of McCarthy has taught an invention as described in claim 1. Please note that lines 2-5 of claim 7 are identical to lines 8-11 of claim 1 and therefore the rejection of that section of claim 7 can be referenced in the rejection of claim 1(g) above. Furthermore, the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, during a next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode. A person of ordinary skill in the art would have recognized that at times, a first processor will only need to transfer a single data word to a second processor. In reality, this single data transfer is merely a load or store instruction. If burst mode were the only available mode, then it would be unproductive for the second processor to prepare itself for a burst transfer (i.e. get ready to increment the memory addresses). In addition, in burst mode, the second processor would still be expecting data to be transferred after the single transfer. This would result in the second processor remaining idle until the first processor indicates that burst mode is over. If a single mode were implemented, the second processor would immediately return to work as soon as the first transfer is over instead of waiting for the first processor's indication that burst mode is over. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a single data transfer mode when the burst mode bit does not indicate burst mode. This would result in a more productive system.

14. Referring to claim 8, Evoy in view of McCarthy has taught an invention as described in claim 1. As described in the rejection of claim 1 above, Evoy has taught a first and second

processor intercoupled by the system address and data buses. In addition, it is well known in the art that processors contain some from of read, write, and chip select signal lines. A person of ordinary skill in the art would have recognized that read and write lines would be used by the first processor to "tell" the second processor whether it will be receiving or transmitting data, respectively. Also, Evoy has taught an enable flag that is used to start and stop the co-processor's operation. Please see Fig.3. The enable flag works the same way as a chip-select line. Basically, the main processor issues an instruction that sets or clears the enable flag (chip select). That value then determines whether or not the co-processor operates.

15. Referring to claim 10, Evoy in view of McCarthy has taught a dual processor system in which data is transferred between two processors. It is noted by the examiner that the only difference between claim 10 and claim 1 is the claiming of an integrated circuit. Evoy has further taught that both processors are on a single integrated circuit. See column 5, lines 52-61 and Fig.2. Therefore, the rejection of claim 10 is based on the same reasons as mentioned above in the rejection of claim 1.

16. Referring to claim 11, Evoy in view of McCarthy has taught an invention as described in claim 10. It is noted by the examiner that the only difference between claim 11 and claim 3 is the claiming of an integrated circuit. Evoy has further taught that both processors are on a single integrated circuit. See column 5, lines 52-61 and Fig.2. Therefore, the rejection of claim 11 is based on the same reasons as mentioned above in the rejection of claim 3.

17. Referring to claim 12, Evoy in view of McCarthy has taught an invention as described in claim 10. It is noted by the examiner that the only difference between claim 12 and claim 4 is the claiming of an integrated circuit. Evoy has further taught that both processors are on a single

integrated circuit. See column 5, lines 52-61 and Fig.2. Therefore, the rejection of claim 12 is based on the same reasons as mentioned above in the rejection of claim 4.

18. Referring to claim 13, Evoy in view of McCarthy has taught an invention as described in claim 10. It is noted by the examiner that the only difference between claim 13 and claim 5 is the claiming of an integrated circuit. Evoy has further taught that both processors are on a single integrated circuit. See column 5, lines 52-61 and Fig.2. Therefore, the rejection of claim 13 is based on the same reasons as mentioned above in the rejection of claim 5.

19. Referring to claim 14, Evoy in view of McCarthy has taught an invention as described in claim 10. It is noted by the examiner that the only difference between claim 14 and claim 6 is the claiming of an integrated circuit. Evoy has further taught that both processors are on a single integrated circuit. See column 5, lines 52-61 and Fig.2. Therefore, the rejection of claim 14 is based on the same reasons as mentioned above in the rejection of claim 6.

20. Referring to claim 15, Evoy in view of McCarthy has taught an invention as described in claim 10. It is noted by the examiner that the only difference between claim 15 and claim 8 is the claiming of an integrated circuit. Evoy has further taught that both processors are on a single integrated circuit. See column 5, lines 52-61 and Fig.2. Therefore, the rejection of claim 15 is based on the same reasons as mentioned above in the rejection of claim 8.

21. Claims 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of McCarthy as applied to claims 1-8 and 10-15 above and in further view of Curran et al., U.S. Patent No. 6,334,179 B1 (herein referred to as Curran).

22. Referring to claim 9, Evoy in view of McCarthy has taught an invention as described in claim 1.

a) Evoy has taught a single memory bank that is accessed by the processor. Evoy has not taught of multiple memory blocks. Curran, on the other hand, has taught the concept of a dual processor system in which multiple memory blocks are implemented. See Fig.1. A person of ordinary skill in the art would have recognized that a plurality of memory banks would replace a single internal memory. A reason for this would be to increase organizational flexibility. For instance, if two memory banks were used, one bank would be used specifically for data and the other for instructions, or something to that effect. Or, in the case of Curran, the use of memory blocks provides increased bandwidth in that each bank can be read or written to at the same time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a plurality of memory blocks as opposed to a single memory block.

b) It should be further noted that if multiple memory blocks were implemented, the processor must be able to access each bank individually. It is well known in the art that each memory bank is assigned a different chip-select address and when that address is applied to each bank, only the bank with that chip-select address will be active. A person of ordinary skill in the art would have recognized that the control word size of the system with the single memory would not have to change to implement multiple memory banks. Instead, in addition to the burst-mode bit field, the upper N bits of the original memory address will become the memory bank chip select address, where $2^N$ = amount of memory banks, and the remaining bits will be used to specify a memory location within the specified bank that will be used as the starting internal address of the data transfer.

c) Once the control register holds the control word written by the first processor, the transfer mode will be determined, the correct memory bank will be selected, and the internal starting bank address will be known. A person of ordinary skill in the art would have recognized that in order to activate a memory bank and determine a starting address, the control register bits must be decoded by the internal address generator logic and applied to the memory bank chip-select and address lines.

23. Referring to claim 16, Evoy in view of McCarthy has taught an invention as described in claim 10. It is noted by the examiner that the only difference between claim 16 and claim 9 is the claiming of an integrated circuit. Evoy has further taught that both processors are on a single integrated circuit. See column 5, lines 52-61 and Fig.2. Therefore, the rejection of claim 16 is based on the same reasons as mentioned above in the rejection of claim 9.

### *Response to Arguments*

24. Applicant's arguments filed on November 25, 2002, have been fully considered but are not deemed to be persuasive.

25. In the remarks, Applicant argues the rejection of claim 1 on pages 7-8, in substance that:

> "Evoy fails to disclose or suggest an "internal memory" (internal to the "second processor"), a "data register" or an "internal address generator" as specified in claim 1. Furthermore, Evoy fails to disclose or suggest any component which 'generates' or 'selects' memory locations for storage of incoming data."

26. This argument is not found persuasive for the following reasons:

a) The Applicant is correct in pointing out that Evoy has not explicitly taught a second processor having its own internal memory. The examiner has confirmed the validity of this contention by originally applying a 35 U.S.C 103 rejection in the previous Office Action instead of a 35 U.S.C.

102 rejection. The original rejection of claim 1(d), as shown above, has stated that the two processors perform data transfers between a single, shared memory source (Fig.2, component 28). However, as previously stated, it would have been obvious to have each processor include its own internal memory to store data/instructions. By having separate memories, bus contention is eliminated, which means a first processor does not have to wait for a second processor to finish accessing memory (as in the case of a single, shared memory). Instead, both processors can access their own respective memories simultaneously, resulting in the minimization of the time required to access memory and also an increase in throughput.

b) In addition, recall the rejection of claim 1(e) from the previous Office Action. It has been stated by the examiner that it is well known in the art that data registers are coupled to the processor's internal memory in order to hold data that is to be retrieved from or written to memory. A data register (register file) is well known to be a fast internal component of a processor. The reason that register memory is very fast is because of its small size and because signals from the CPU do not have to propagate long distances to reach the registers (with respect to cache, main memory, hard-disk, etc.). For Applicant's benefit, readings have been attached. Hennessy and Patterson, <u>Computer Architecture - A Quantitative Approach</u>, 2nd Edition, 1996, shows that registers are a well-known form of memory internal to the CPU. See Fig.1.15, Fig.1.16, and page 71. Hennessy also shows that the data register file is coupled to a memory as stated by the examiner in the previous Office Action. See Fig 3.1 on page 130.

c) Finally, with regards to the internal address generator, recall the rejection of claim 1(f) in the previous Office Action. The examiner has stated that an internal address generator would be coupled to the control register and also to the memory in order to decode the address held in the

program counter and access the correct memory address. It has been explained by Applicant and noted by the examiner that the purpose of Applicant's internal address generator is to utilize a control word supplied by the main processor in order to generate memory locations in which incoming data will be stored (from page 7 of the remarks). It follows that this type of component would inherently exist within Evoy's system. The program counter (PC), which is part of the overall control register arrangement, according to column 5, lines 1-7 of Evoy, is used to store a starting address that has been specified and written by the main processor. See column 8, lines 27-31. It is well known in the art that a PC is incremented after a memory access is performed with the current address held in the PC. This increment is inherently performed by arithmetic logic, which adds a specified amount to the PC each time, and overwrites the PC's current contents (current address) with the newly obtained result (next address). This operation can also be seen in Fig.5 of Evoy in that step 116 (retrieval of a next instruction) can be performed multiple times (as denoted by the arrow from step 122 to step 114). If the coprocessor's operation includes fetching multiple instructions, then it must include logic that generates new addresses for the PC. The reason it is inherent for an "internal address generator" to be coupled to the control register (which includes the PC) and internal memory is that it needs to be able to "grab" the current address from the PC, and add a specified amount to the PC so that the result can be used to access the next location in memory. In addition, the address is "decoded" in a sense before being applied to the internal memory, where decoding is meant to be a type of translation. In this case, the internal address generator will take the address, along with enable and read/write data, and turn it into a group of signals that will be used to enable the memory and then perform a certain operation on the memory at the specified address. For Applicant's

benefit, readings have been attached. Kenneth L. Short, Microprocessors and Programmed Logic, 1981, shows the basics of a program counter (PC) and that it must be incremented to point to the next memory address. It should be recognized that an "internal address generator" would be used to generate new PC addresses by incrementing the current address.

27. It has been noted by the examiner that all remaining arguments by Applicant (pages 8-9 of the remarks) involve the contention that Evoy, McCarthy, and Curran have not taught an internal memory to the second processor, a data register, and an internal address generator. However, from the explanations above, it should be realized that the rejections set forth in the previous Office Action stand as valid.

### *Conclusion*

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
December 12, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100